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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2676	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,485	BOOTH, LAWRENCE A.	
	Examiner	Art Unit	
	Joni Hsu	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, and 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Dulong (US005825921A).

3. With regard to Claim 1, Dulong describes an apparatus comprising a display controller (419, Figure 5); an internal frame buffer (30) coupled to the display controller; and a control circuitry (416) to copy display data from an external frame buffer (615) to the internal frame buffer, wherein the display data copied into the internal frame buffer is the same display data read by the display controller from the external frame buffer (Col. 13, lines 11-21; Col. 3, lines 6-23; Col. 42, lines 14-22).

4. With regard to Claim 2, Dulong describes that the display data is copied into the internal frame buffer (30, Figure 5) simultaneously with the display controller (419) reading the display data from the external frame buffer (615) (Col. 42, lines 55-63).

5. With regard to Claim 5, Dulong describes that the display controller (419, Figure 5), the internal frame buffer (30) and the control circuitry (416) are disposed on a single graphics chip (525) and the external frame buffer (615) is disposed on another chip separate from the graphics chip (Col. 13, lines 11-21).

6. With regard to Claim 6, Dulong describes that the display controller (419, Figure 5), the internal frame buffer (30) and the control circuitry (416) are disposed on a single processor chip (525) (Col. 13, lines 11-21).

7. With regard to Claim 7, Dulong describes that the control circuitry (416, 418) comprises at least one register to hold at least one data transaction of display data (Col. 15, line 66-Col. 16, line 40).

8. Thus, it reasonably appears that Dulong describes or discloses every element of the Claims 1, 2, and 5-7 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 3, 4, 9-11, 13, 16, 17, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dulong (US005825921A) in view of Schinnerer (US 20030227460A1).

12. With regard to Claim 3, Dulong is relied upon for the teachings as discussed above relative to Claim 1. Dulong describes that double buffering is performed using an internal frame buffer (30, Figure 5) and an external frame buffer (615), and the display controller (419) reads the display data from the internal frame buffer (Col. 13, lines 11-21; Col. 3, lines 6-23; Col. 42, lines 14-22).

However, Dulong does not teach that the display controller reads the display data from the internal frame buffer until the display controller receives a signal indicating that the external frame buffer contains the most recent display data. However, Schinnerer describes double buffering [0012] and a buffer swap is performed when the display controller (50, Figure 2) receives a signal indicating that the output frame buffer contains the most recent display data [0074, 0070]. The same image frame is repetitively transmitted until a buffer swap is performed [0038]. In other words, the display controller reads the display data from the input frame buffer

[0029, 0032] until the display controller receives a signal indicating that the output frame buffer contains the most recent display data, then a buffer swap is performed [0074, 0070, 0038].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Dulong so that the display controller reads the display data from the internal frame buffer until the display controller receives a signal indicating that the external frame buffer contains the most recent display data as suggested by Schinnerer because Schinnerer suggests that this must be done so that the most recent display data can be copied into the input frame buffer so that the data being read from the input frame buffer will be updated [0032, 0038, 0074].

13. With regard to Claim 4, Dulong describes that double buffering is performed using an internal frame buffer (30, Figure 5) and an external frame buffer (615), and the display controller (419) reads the display data from the internal frame buffer (Col. 13, lines 11-21; Col. 3, lines 6-23; Col. 42, lines 14-22).

However, Dulong does not teach that the display controller reads the display data from the internal frame buffer at least one time after a new frame display refresh operation. However, Schinnerer describes double buffering [0012] and that the display controller (50, Figure 2) reads the display data from the input frame buffer [0029, 0032, 0038] at least one time after a buffer swap or a new frame display refresh operation [0074, 0070, 0038].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Dulong so that the display controller reads the display data from the internal frame buffer at least one time after a new frame display refresh operation as

suggested by Schinnerer because Schinnerer suggests that after a new frame display refresh operation, the input frame buffer has the most recent display data and the data can then be read out of the input frame buffer [0029, 0032, 0038, 0074, 0070].

14. With regard to Claim 9, Dulong describes a system (500, Figure 2) comprising a processor (510); a display device (518) (Col. 8, line 55-Col. 9, line 17); a graphics chip (525) coupled between the processor and the display device (Col. 10, lines 5-10), the graphics chip including a display controller (419, Figure 5), an internal memory array (30) and data copy circuitry (416); and an external memory array (615) disposed on another chip separate from the graphics chip, wherein the data copy circuitry is coupled between the external memory array and the internal memory array to enable data from the external memory array to be copied to the internal memory array (Col. 13, lines 11-21; Col. 3, lines 6-23; Col. 42, lines 14-22).

However, Dulong does not teach that data is copied from the external memory array to the internal memory array during a new frame display refresh operation, wherein subsequent display refresh operations are accomplished by the display controller retrieving data from the internal memory array until a new frame is available in the external memory array. However, Schinnerer describes double buffering [0012] and that data is copied from the output memory array to the input memory array during a buffer swap or a new frame display refresh operation [0070]. The same image frame is repetitively transmitted until a buffer swap is performed [0038]. In other words, subsequent display refresh operations are accomplished by the display controller (50, Figure 2) retrieving data from the input memory array [0029, 0032] until a new

frame is available in the output memory array, then a buffer swap is performed [0074, 0070, 0038]. This would be obvious for the same reasons given in the rejection for Claim 3.

15. With regard to Claim 10, Dulong describes that the display controller (419, Figure 5) retrieves the data from the external memory array (615) simultaneously with copy of the data from the external memory array to the internal memory array (30) (Col. 42, lines 55-63).

16. With regard to Claim 11, Dulong describes that the display data copied into the internal memory array (30, Figure 5) is the same display data read by the display controller (419) from the external memory array (615) (Col. 13, lines 11-21; Col. 3, lines 6-23; Col. 42, lines 14-22).

17. With regard to Claim 13, Claim 13 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

18. With regard to Claim 16, Dulong describes a method comprising reading display data from an external frame buffer (615, Figure 5) by a display controller (419); and loading the same display data from the external frame buffer to an internal frame buffer (30) (Col. 13, lines 11-21; Col. 3, lines 6-23; Col. 42, lines 14-22).

However, Dulong does not teach that the display data is read from the external frame buffer during a new frame display refresh operation; and loading the display data from the external frame buffer to an internal frame buffer during the new frame display refresh operation. However, Schinnerer describes double buffering [0012], and a method comprising reading

display data from an output frame buffer by a display controller (50, Figure 2) during a buffer swap or a new frame display refresh operation; and loading the same display data from the output frame buffer to an input frame buffer during the new frame display refresh operation [0074, 0070]. This would be obvious for the same reasons given in the rejection for Claim 3.

19. With regard to Claim 17, Dulong describes that double buffering is performed using an internal frame buffer (30, Figure 5) and an external frame buffer (615), and the display controller (419) reads the display data from the internal frame buffer (Col. 13, lines 11-21; Col. 3, lines 6-23; Col. 42, lines 14-22).

However, Dulong does not teach determining if a new frame is available in the external frame buffer; and reading the display data in the internal frame buffer by the display controller during subsequent display refresh operations if a new frame is not available in the external frame buffer. However, Schinnerer describes double buffering [0012] and performing a buffer swap when the display controller (50, Figure 2) determines that a new frame is available in the output frame buffer [0074, 0070]. The same image frame is repetitively transmitted until a buffer swap is performed [0038]. In other words, Schinnerer describes determining if a new frame is available in the output frame buffer [0074, 0070]; and reading the display data in the input frame buffer by the display controller [0029, 0032] during subsequent display refresh operations if a new frame is not available in the output frame buffer.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Dulong to include determining if a new frame is available in the external frame buffer; and reading the display data in the internal frame buffer by the display

controller during subsequent display refresh operations if a new frame is not available in the external frame buffer as suggested by Schinnerer. Schinnerer suggests that this must be done so that the most recent display data can be copied into the input frame buffer so that the data being read from the input frame buffer will be updated. If no new frame is available in the output frame buffer, then that means that the data in the input frame buffer is still the most recent, and it can keep on being read [0032, 0038, 0074].

20. With regard to Claim 19, Claim 19 is similar in scope to Claim 10, and therefore is rejected under the same rationale.

21. With regard to Claim 20, Dulong describes that the loading of the data from the external frame buffer (615, Figure 5) to the internal frame buffer (30) is accomplished using data copy circuitry (416) (Col. 13, lines 11-21; Col. 3, lines 6-23; Col. 42, lines 14-22).

22. With regard to Claim 21, Claim 21 is similar in scope to Claim 5, and therefore is rejected under the same rationale.

23. With regard to Claim 22, Dulong describes that loading of the data from the external frame buffer (615, Figure 5) to the internal frame buffer (30) (Col. 13, lines 11-21; Col. 3, lines 6-23; Col. 42, lines 14-22) further comprises temporarily storing at least one data transaction of the display data in a register (Col. 15, line 66- Col. 16, line 40). The data is read from the external frame buffer and written into the internal frame buffer (Col. 13, lines 11-21; Col. 3, lines

6-23; Col. 42, lines 14-22), so writing the stored data into the internal frame buffer is inherently based on an external memory read signal.

24. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dulong (US005825921A) in view of Reitmeier (US006118486A).

Dulong is relied upon for the teachings as discussed above relative to Claim 1. Dulong describes that the control circuitry (416, Figure 5) reads data from an external memory (615) and writes the data into an internal memory frame buffer (30) (Col. 13, lines 11-21; Col. 3, lines 6-23; Col. 42, lines 14-22), so the control circuitry must inherently generate a write signal to be used by the internal frame buffer based on an external memory read signal.

However, Dulong does not that the control circuitry is to generate a write signal to be used by the internal frame buffer also based a memory clock signal. However, Reitmeier describes double buffering (Col. 5, line 59-Col. 6, line 16) and that the control circuitry (200, Figure 1) is to generate a write signal to be used by the output frame store buffer (164) based on a memory clock signal (Col. 6, line 61-Col. 7, line 8).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Dulong so that the control circuitry is to generate a write signal to be used by the internal frame buffer also based on a memory clock signal as suggested by Reitmeier because Reitmeier suggests that this is needed in order to ensure the correct frequency for the graphics format (Col. 1, lines 47-51; Col. 6, lines 4-14).

25. Claims 12, 15, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dulong (US005825921A) in view of Schinnerer (US 20030227460A1), further in view of Aleksic (US 20040150647A1).

26. With regard to Claim 12, Dulong and Schinnerer are relied upon for the teachings as discussed above relative to Claim 9.

However, Dulong and Schinnerer do not teach a graphics generator disposed on the graphics chip. However, Aleksic describes a system comprising a processor (114, Figure 2); a display device (130); a graphics chip (117) coupled between the processor and the display device [0013-0014], the graphics chip including an internal memory array (360) [0018]; and an external memory array (112) disposed on another chip separate from the graphics chip [0034]. Aleksic also describes double buffering [0035]. Aleksic also describes a graphics generator (118) disposed on the graphics chip [0018].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Dulong and Schinnerer to include a graphics generator disposed on the graphics chip as suggested by Aleksic because Aleksic suggests that a graphics generator is needed to render received image data into rendered image data, or display data [0018].

27. With regard to Claim 15, Dulong and Schinnerer do not teach a portable power source coupled to power the display controller, the internal memory array, the external memory array

and the data copy circuitry. However, Aleksic describes a portable power source (125) coupled to power the system [0015].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Dulong and Schinnerer to include a portable power source coupled to power the display controller, the internal memory array, the external memory array and the data copy circuitry as suggested by Aleksic because Aleksic suggests that portable power sources are needed for many handheld devices, such as personal digital assistants and mobile phones [0003-0004].

28. With regard to Claim 18, Dulong and Schinnerer do not teach that the display data from the external frame buffer includes rendered graphics objects or an entire frame. However, Aleksic describes that the display data from the external frame buffer includes rendered graphics objects or an entire frame [0018].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Dulong and Schinnerer so that the display data from the external frame buffer includes rendered graphics objects or an entire frame as suggested by Aleksic. Aleksic suggests that the amount of rendered graphics objects to be stored is generally larger than the size of memory available internal to the graphics system. Accordingly, in conventional systems, the rendered image data is stored in other memory external to the graphics system [0018].

29. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dulong (US005825921A) in view of Schinnerer (US 20030227460A1), further in view of Reitmeier (US006118486A).

Claim 14 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella can be reached on 571-272-7778. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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